High-Efficiency Differential RF Front-End for a Gen2 RFID Tag

Peng Wei, Wenyi Che, Zhongyu Bi, Chen Wei, Yan Na, Li Qiang, and Min Hao

***Abstract*—This brief proposes the analysis and design of a high-efficiency differential radio-frequency (RF) front-end for electronic-product-code second-generation-compatible RF identification tags. By studying the operating mechanism of an N-stage rectifier using a dynamic compensation technique, we propose a steady-state model to predict its output voltage and power conversion efficiency (PCE). The model gives insight to specify circuit parameters according to different input and load conditions. To compose the RF front-end, the rectifier is designed along with an envelope detector, a voltage regulator, and a backscattering modulator. The RF front-end is implemented in 0.18-μm standard complementary metal–oxide–semiconductor technology with electrically erasable programmable read-only memory. Both simulation and measurement results verify the proposed steady-state model. The maximum PCE of the RF front-end reaches 43% at −17-dBm incident power.**

***Index Terms*—Power conversion efficiency (PCE), radio-frequency (RF) front-end, rectifier, second-generation (Gen2) radio-frequency identification (RFID) tag, steady-state model.**

I. Introduction

LONG-RANGE ultrahigh-frequency radio-frequency identification (RFID) has been widely used in many fields. The passive manner of RFID requires a tag to convert reader's interrogating power for system supply. According to Friis's transmission equation in free space, the operating power of tag $P_{\rm tag}$ [1] is calculated as follows:

$$P_{\rm tag} = {\rm EIRP}_{\rm reader} \cdot G_{\rm tag} \cdot \eta_{\rm rectifier} \cdot \left(\frac{\lambda}{4\pi d}\right)^2 \qquad (1)$$

where ${\rm EIRP}_{\rm reader}$ is the effective isotropic radiation power of a reader, $G_{\rm tag}$ is the tag antenna gain, $\eta_{\rm rectifier}$ is the RF-to-direct-current (dc) power conversion efficiency (PCE) of a rectifier, and d is the READ range. As ${\rm EIRP}_{\rm reader}$ is defined by radio regulations, the READ range of an RFID system is directly determined by a tag's PCE.

In order to increase the tag's PCE at a low incident power level, rectifiers using threshold compensation techniques were introduced in the past years. The early generation of threshold compensation techniques is called static compensation [3], [8], [9]. In these circuits, static voltage biases are generated to lower the turn-on threshold and the forward voltage drop of the rectifiers' passing devices. The typical PCE value of a static compensated rectifier is 36.6% at 4 m [8]. The major drawback of a static compensated rectifier is its inevitable leakage current during the negative phase. As RFID evolution continues, it becomes the bottleneck in PCE enhancement. Several studies report a four-transistor cell that uses dynamic threshold compensation [1], [2]. Using a complementary control mechanism, reverse leakage current is minimized in these circuits. The PCE of a dynamic compensated rectifier reaches as high as 67.5% at a −12.5-dBm incident power level [1].

Compared with the integrated analytical system of the static compensation technique, the study of a dynamic compensation technique is insufficient. In the first place, PCE optimization methods for different input and load conditions are meaningful for circuit design. Furthermore, reports on the design of whole differential RF front-ends with a dynamic compensated rectifier, a demodulator, and a voltage regulator are few in the literature.

By studying the circuit mechanism of a dynamic compensated rectifier, we propose a steady-state model in a mathematical way through which a design flow for circuit design is proposed. The impact of the stage number N, the device dimension W/L, and a load circuit is revealed. On the other hand, functional circuits such as an active envelope detector and a voltage regulator are designed to compose an RF front-end. Using the analytical model, optimization of the rectifier is carried out according to real circuit conditions. Test results of the RF front-end are given at the end of this brief.

II. Rectifier Analysis

In Fig. 1, an N-stage dynamic compensated rectifier based on a four-transistor cell is shown. Here, the study on this rectifier starts from a single-stage topology and is extended to an N-stage situation, including the output voltage V_o and the corresponding PCE.

In the situation of a tag, the load capacitor of the rectifier is designed to be large so as to smoothen the output voltage and reduce the output voltage drop when modulated signals are transferred to the rectifier. Under this circumstance, the intrinsic setup mechanism of the rectifier could be ignored, and

Manuscript received July 22, 2010; revised December 1, 2010; accepted January 31, 2011. Date of current version April 20, 2011. This work was supported in part by the Open Fund of the State Key Laboratory of Application-Specific Integrated Circuit and System, China, under Grant 09KF006 and in part by the General Project of the State Key Laboratory of Application-Specific Integrated Circuit and System, China, under Grant 09MS009. This paper was recommended by Associate Editor J. Paramesh.

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Digital Object Identifier 10.1109/TCSII.2011.2124530

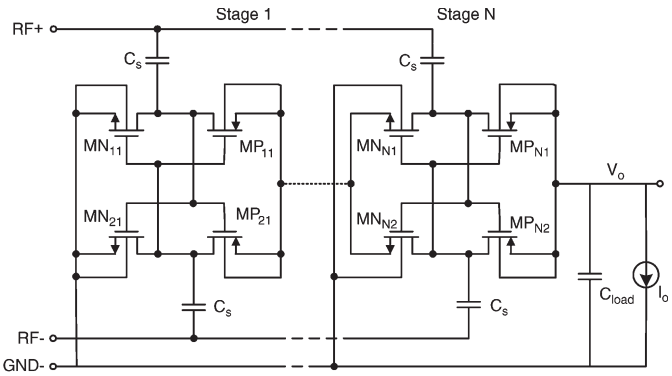

Fig. 1. N-stage differential rectifier circuit.

the analysis of the transistors is based on the steady state when V_o is set up and remains stable.

A. Output Voltage

Fig. 2(a) shows the single-stage rectifier. Its load includes the load storage capacitor $C_{\rm load}$ and the dc I_o (i.e., the equivalent load of the other circuits). Since the circuit topology is fully symmetric, MP_1 is chosen for analysis. According to the transistor operating state of MP_1, we divide a cycle into six regions. The voltage and current waveforms of the transistors in one complete cycle are shown in Fig. 2(b), including operating region partition. With the steady-state assumption, the voltage of nodes x and y is added to the dc offset $V_{o1}/2$.

According to our assumption, the charge stored in $C_{\rm load}$ remains stable during an operating cycle. Therefore, the current consumed on I_o is equal to the charging current of MP_1 and MP_2 as follows:

$$I_o = \overline{I_{\rm MP_1} + I_{\rm MP_2}} = \frac{Q_{\rm total}}{T} \tag{2}$$

which could be replaced as follows:

$$I_o = \frac{2}{T}(Q_{\rm sat1} + Q_{\rm linear} + Q_{\rm sat2} + Q_{\rm sub1} + Q_{\rm leakage} + Q_{\rm sub2}) \tag{3}$$

where $Q_{\rm sat1}$, $Q_{\rm sat2}$, $Q_{\rm sub1}$, $Q_{\rm sub2}$, $Q_{\rm linear}$, and $Q_{\rm leakage}$ denote the charge flowing through MP_1 in each operating regions. The detailed analysis is shown as follows.

1) In region A $[t_1,\ t_2]$, as depicted in Fig. 2(b), $|V_{gs}|$ of MP_1 increases after t_0. At t_1, the metal–oxide–semiconductor (MOS) transistor MP_1 begins to conduct in the strong inversion region. The current in the saturation region is as follows:

$$I_{ds} = \frac{1}{2}\mu_o C_{\rm ox}\frac{W}{L}(V_{gs} - V_{\rm th})^2(1 + \lambda V_{ds}). \tag{4}$$

Therefore, $Q_{\rm sat1}$ is given by

$$Q_{\rm sat1} = -\int_{t_1}^{t_2} \frac{1}{2}\mu_0 C_{\rm ox}\frac{W}{L}\left(V_{o1} - V_{\rm iy} - |V_{\rm thp1}|\right)^2 \times \left[1 + \lambda\left(V_{o1} - V_{\rm ix}\right)\right] dt \tag{5}$$

where $V_{\rm thp1}$ is the threshold voltage of MP_1 without a body effect, $V_{\rm ix}$ and $V_{\rm iy}$ are the voltage of nodes x and y (here, we assume that $V_{\rm ix}$ and $V_{\rm iy}$ are sinusoidal waveforms with a frequency of f_0).

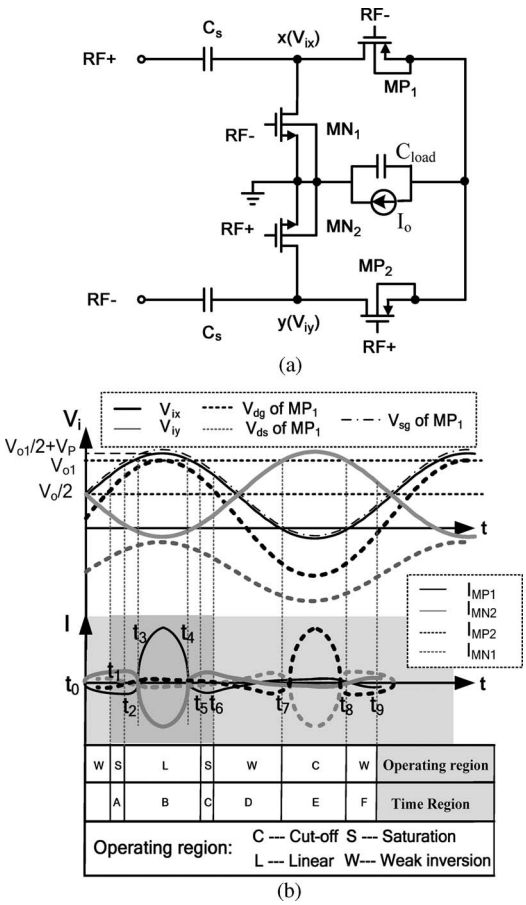

Fig. 2. (a) Single-stage topology of the rectifier. (b) Voltage and current curve of MOS transistors.

2) In region B $[t_2,\ t_5]$, After t_1, the difference between $|V_{gs}|$ and $|V_{ds}|$ decreases. At t_2, MP_1 enters the linear region. The current in the linear region is given by

$$I_{ds} = \mu_0 C_{\rm ox}\frac{W}{L}\left(V_{gs} - V_{\rm th} - \frac{1}{2}V_{ds}\right)V_{ds}. \tag{6}$$

As shown in Fig. 2(b), the current direction switches at t_2 because the equivalent source of MP_1 changes at that point. The body effect is also considered here for the static connect of a substrate. The threshold voltage [10] is given by

$$V_{\rm thp2} = V_{\rm thp1} + K_1\left(\sqrt{\Phi_s - V_{\rm bs}} - \sqrt{\Phi_s}\right) + K_2 V_{\rm sb} \tag{7}$$

where $V_{\rm thp2}$ is the threshold voltage when a substrate is connected to a lower voltage than than the source. The charge quantity in this region is given by

$$Q_{\rm linear} = -2\int_{t_2}^{t_3}\mu_0 C_{\rm ox}\frac{W}{L}\left[V_{o1} - V_{\rm iy} - |V_{\rm thp1}| - \frac{1}{2}(V_o - V_{\rm ix})\right] \times \left(\frac{V_{o1}}{2} - V_p\sin(\omega t)\right)dt + \int_{t_3}^{t_4}\mu_0 C_{\rm ox}\frac{W}{L} \times \left[2V_p\sin(\omega t) - |V_{\rm thp2}| - \frac{1}{2}\left(V_p\sin(\omega t) - \frac{V_{o1}}{2}\right)\right]dt. \tag{8}$$

3) Region C $[t_5, t_6]$ is a similar region with Region A. The charge expression is given by

$$Q_{\text{sat2}} = -\int_{t_5}^{t_6} \frac{1}{2}\mu_0 C_{\text{ox}} \frac{W}{L}\left[\frac{V_{o1}}{2} + V_p \sin(\omega t) - |V_{\text{thp1}}|^2\right] \times \left\{1 + \lambda\left[\frac{V_{o1}}{2} - V_p \sin(\omega t)\right]\right\} dt. \quad (9)$$

4) In region D $[t_6, t_7]$, after t_6, MP_1 enters the weak inversion region. The current between the drain and the source referred is given by [10]

$$I_{ds} = I_{s0}\left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right]\exp\left(\frac{V_{gs} - V_{\text{th}} - V_{\text{off}}}{n v_t}\right) \quad (10)$$

with

$$I_{s0} = \mu_0 \frac{W}{L}\sqrt{\frac{q\varepsilon_{si} N_{\text{ch}}}{2\Phi_s}} v_t^2. \quad (11)$$

Therefore,we could get Q_{sub1} as follows:

$$Q_{\text{sub1}} = -\int_{t_6}^{t_7} I_{s0}\left[1 - \exp\left(\frac{V_{o1} - 2V_p \sin(\omega t)}{2v_t}\right)\right] \times \exp\left[\frac{V_{o1} + 2V_p \sin(\omega t) - 2|V_{\text{thp1}}| - 2V_{\text{off}}}{2n v_t}\right] dt. \quad (12)$$

5) In region E $[t_7, t_8]$, after t_7, the value of V_{dg} and V_{sg} is both below 0, and MP_1 enters the cutoff region. Although the leakage current of this region is small after optimization, it is still considered for the accuracy of the model. The expression of leakage current [10] is given by

$$I_{ds} = I_{s0}\left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right]\exp\left(\frac{-V_{\text{th}} - V_{\text{off}}}{n v_t}\right). \quad (13)$$

Therefore, Q_{leakage} in this region is given by

$$Q_{\text{leakage}} = \int_{t_7}^{t_8} I_{s0}\left[1 - \exp\left(-\frac{2V_p \sin(\omega t) - V_{o1}}{2v_t}\right)\right] \times \exp\left(\frac{-|V_{\text{thp2}}| - V_{\text{off}}}{n v_t}\right). \quad (14)$$

6) In region F $[t_8, t_9]$, At t_8, MP_1 enters the weak inversion region again, and this state lasts until t_9. Therefore,Q_{sub2} is given by

$$Q_{\text{sub2}} = -\int_{t_8}^{t_9} I_{s0}\left[1 - \exp\left(-\frac{V_{o1} - 2V_p \sin(\omega t)}{2v_t}\right)\right] \times \exp\left(\frac{V_{o1} + 2V_p \sin(\omega t) - 2|V_{\text{thp1}}| - 2V_{\text{off}}}{2n v_t}\right) dt. \quad (15)$$

By combining the equations from (4)–(17), we could get a function as follows:

$$V_{o1} = f\left(\frac{w}{L}, R_L, V_p\right) \quad (16)$$

where I_o is replaced by the equivalent resistor R_L, which is equal to V_{o1}/I_o. Equation (16) shows that the output voltage V_{o1} is a function with three independent variables, i.e., W/L, R_L, and V_p. V_{o1} of a single stage can be got by solving (16).

In cascaded structures, the behavior of the Nth stage is similar to that of stage 1. If we define the voltage shift of the Nth stage by V_{oN}, the output voltage of the rectifier is given by

$$V_o = V_{o1} + V_{o2} + \cdots + V_{oN}. \quad (17)$$

B. PCE

PCE is defined as the ratio of output dc power and incident RF power as follows:

$$\eta = \frac{P_{\text{dc}}}{P_{\text{in}}} = \frac{P_{\text{dc}}}{P_{\text{dc}} + P_{\text{loss}}} \quad (18)$$

where P_{loss} is the power loss of the rectifier circuit itself.

The output dc power of the rectifier is as follows:

$$P_{\text{dc}} = I_o V_o. \quad (19)$$

The power dissipation P_{loss} can be calculated by summing up the power loss of the rectifier. It is given by

$$P_{\text{loss}} = P_{\text{sub}} + P_{\text{sat}} + P_{\text{linear}} + P_{\text{leakage}} \quad (20)$$

where P_{sub}, P_{sat}, P_{linear}, and P_{leakage} represent the power dissipation in the different operation region of MOS transistors and can be represented by the integration of I_{ds} multiplied by V_{ds}.

The overall PCE is given by

$$\eta = \frac{P_{\text{dc}}}{P_{\text{dc}} + N\left(P_{\text{sub}} + P_{\text{sat}} + P_{\text{linear}} + P_{\text{leakage}}\right)} \times 100\%. \quad (21)$$

C. Discussions

The joint effect of the stage number N, the transistor dimension W/L, and the equivalent resistor R_L is concluded in (16) and (21). Iteration, together with other mathematical methods, is used here to get approximate solutions for these transcendental equations. Based on these equations, Fig. 3(a)–(f) are plotted along with the simulation results obtained using the Berkeley short-channel insulated-gate field-effect transistor (FET) model 3V3.3 [10].

In Fig. 3(a) and (b), the curve of V_o and PCE is plotted as a function of the stage number N. As depicted in Fig. 3(a), the increase in N causes higher V_o at a larger input region and lower V_o at a smaller input region. In Fig. 3(b), the increase in N causes the right shift of the optimal PCE region and the lowering of peak PCE. In a multistage topology, parallel input impedance causes smaller resonant V_p, which makes the bias of the transistors hard to overcome a large turn-on threshold and the V_o and PCE hard to achieve. While in the large input region, the signal amplitude is large enough compared with the threshold, and the multistage rectifier can reach high V_o and PCE for the cascade topology. Therefore, the turning point in the V_o curve and the shift of the optimal PCE region is formed. The drop of peak PCE in the multistage rectifier is mainly caused by the body effect, which causes a larger V_{th} of n-channel MOS (nMOS) in higher stages and shorter charging time in a time period.

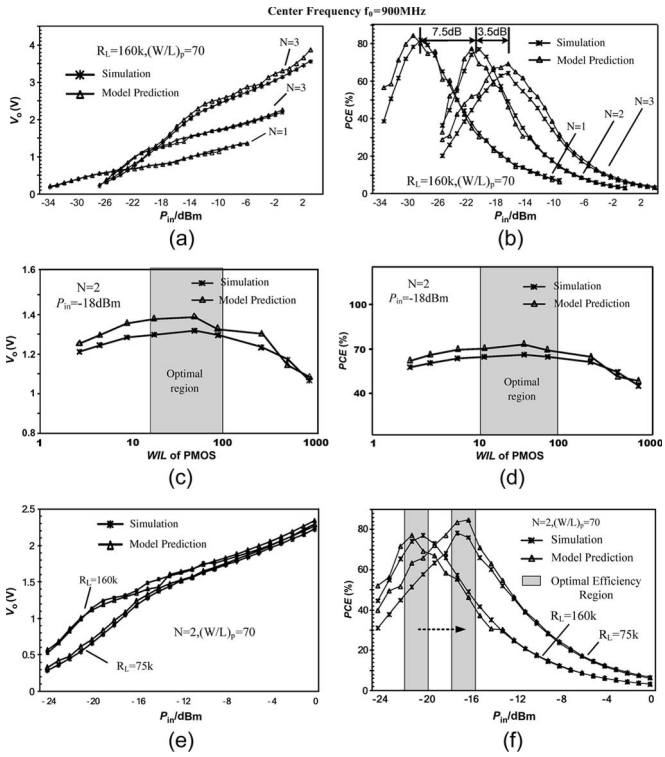

Fig. 3. (a), (c), and (e) are V_o of different N, W/L, and R_L, respectively. (b), (d), and (f) are the PCE of different N, W/L, and R_L, respectively.

In Fig. 3(c) and (d), the impact of the transistor dimension W/L is shown. Small W/L will increase the equivalent resistor of the transistors to be larger, which causes both low conducting capability and an extremely large real part of input impedance. On the contrary, large W/L could bring large gate capacitance. Consequently, the series capacitor from nodes x and y to the ground will lower the amplitude of $V_{\rm ix}$ and $V_{\rm iy}$, reducing V_o and PCE. Under a typical condition of a 160-kΩ load resistor and $P_{\rm in}$ of -18 dBm, the optimal PCE region of a two-stage rectifier lies in the medium of 30–100.

In Fig. 3(e) and (f), different R_L is used for a two-stage rectifier. Smaller R_L leads to lower V_o and the right shift of the optimal PCE region. High voltage can be achieved more easily with equal current and large R_L, which make the optimal PCE region of larger R_L moves to the left.

Here, we must figure out that in both lower and higher regions, there is a steep drop of PCE. That is because, in a low-power region, MOSFETs work basically in the subthreshold region, which allows small forward current. Whereas in the large power region, the drop of PCE is mainly caused by the increment of reverse current.

A brief design flow of the rectifier could be inferred from the aforementioned analysis as follows.

1) Specify the targeting sensitivity (i.e., lowest operable incident power) $P_{\rm in}$ for the tag.
2) After designing the analog, digital, and memory circuits in the tag, calculate the load resistance R_L according to the real load I–V curve.
3) Choose the right stage number N for V_o, which is the supply voltage level of the whole tag system. Minimal N should be selected as the degradation of peak PCE in the multistage rectifier.

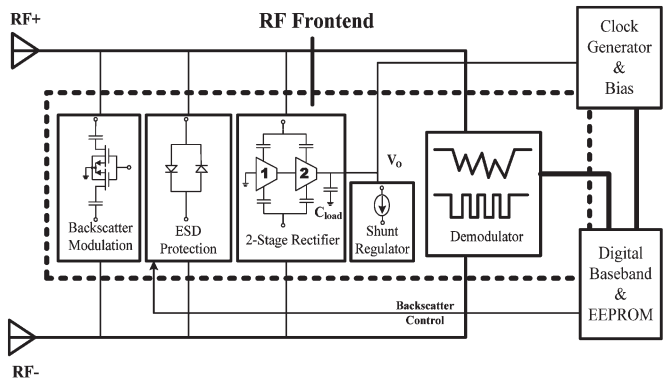

Fig. 4. Differential RF front-end architecture.

4) Select the suitable transistor dimension (W/L) to make the optimal PCE region located around the required sensitivity. Meanwhile, chip size and input impedance should also be considered.
5) Find the corresponding PCE around the sensitivity level. Check whether it is sufficient; if it is not, modify the sensitivity specification, and go back to step 3 to repeat the course.

III. Circuit Design

A. System Architecture

Fig. 4 shows the architecture of the differential RF front-end.

A two-stage four-transistor cell is utilized here to meet the system specification, rendering both the high voltage supply and the efficiency of the front-end. A shunt regulator is used to limit the peak output voltage of the rectifier. A differential envelope detector is also introduced to extract the digital data bit stream from an RF signal to the digital baseband. A modulation module and an electrostatic discharge (ESD) protection circuit are also included in the RF front-end.

B. Two-Stage Rectifier

According to the design flow, we specify the targeting sensitivity to -18 dBm and the equivalent R_L to 160 K, considering the load condition of the rectifier. The optimal PCE region locates in the power region from -20 to -15 dBm. Therefore, we choose the two-stage topology to meet the demand. The W/L of p-channel MOS (pMOS) is 70, and the dimension ratio between PMOS and NMOS is about 2.3 to make their charging capability balance. The length of the transistors is the minimal length limited by technology because small length introduce little parasitic capacitance, which will lower the PCE of the rectifier.

C. Demodulator

The front-end circuit uses an incoherent detector to demodulate forward-link amplitude-shift-keyed signals. The cascaded stages of an envelope extractor, a low-pass filter, and a hysteresis comparator compose the circuit. Fig. 5 shows the diagram. The operating mechanism of the envelope extractor is similar to that of the rectifier. It employs a static $V_{\rm th}$ compensation method (i.e., theVC blocks shown in Fig. 5) for envelope extraction and amplification.

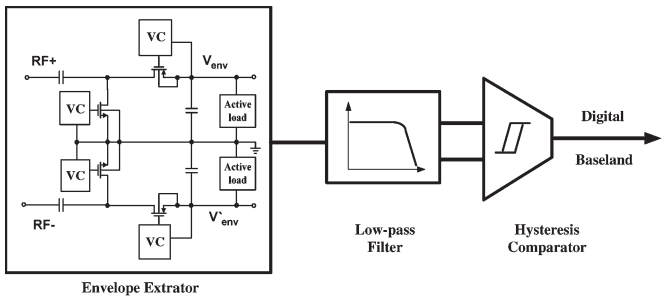

Fig. 5. Demodulator.

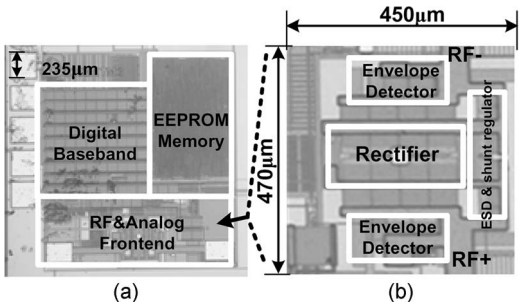

Fig. 6. (a) Tag chip micrograph. (b) RF front-end micrograph of the tag shown in (a).

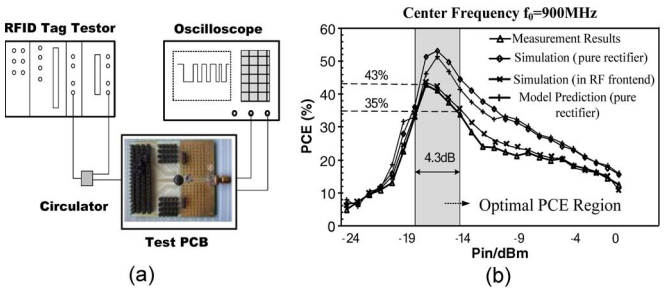

Fig. 7. (a) Test environment of the tag. (b) Comparison among test, simulation, and model results.

IV. Experimental Results

A. Chip Fabrication

The front-end is designed and fabricated as a part of a tag chip in 0.18-μm standard CMOS technology with with electrically erasable programmable read-only memory. Fig. 6 shows the micrograph of the chip. As depicted in Fig. 6(b), the layout topology of the rectifier and the envelope detector is symmetrical for performance consideration. As shown in Fig. 7(a), the chip is tested on a printed circuit test board in a chip-on-board package. The RF power is provided by a NI RFID tag tester (PXI-1042Q).

B. Measurements

The tag chip is verified to have a correct second-generation (Gen2) communication function with the NI tester. The front-end is tested using a real tag circuit as its load.

During the test, power losses introduced by the testing environment and devices have been taken into consideration, including the chip package, the test board, the balun, the circulator, the cables, and the matching network. The evaluations of all kinds of losses have been listed in Table I. After decapping, measurement results are depicted in Fig. 7, along with the model prediction and simulation results. Measurement results show that at -17-dBm input power (i.e., center frequency equals 900 MHz), the peak PCE is 43%. At this point, the input impedance of the RF front-end is $17.2 - j98.8\ \Omega$. The region where PCE is above 35% locates in -18.5–-14.2 dBm, with a 4.3-dB span, which is basically consistent with our design target.

TABLE I
Loss Evaluations of the Test Environment

Factors	Power Loss	PCE loss(@-17dBm)
Package and Test board	0.2dB	1.7%
Balun	0.8dB	6%
Matching Network	0.2dB	1.7%
Cables and circulator	0.5dB	3.5%
Total	1.7dB	12.9%

TABLE II
Comparison of PCE in Recent Studies

Ref.	Technology	V_{th} Compensation Technique	P_{in} (dBm)	$I_0(\mu A)$/ $V_0(V)$	Peak PCE (%)
[1]*	0.18 μm CMOS	dynamic	-12	61.6/0.62	67.5
[8]	0.35μm CMOS with FeRAM	static	---	---	36.6
[9]*	0.35μm CMOS	static	-9.9	---	29
This work	0.18 μm CMOS with EEPROM	dynamic	-17	4.2/0.7	43

* Pure rectifier implementation is proposed and other works are based on an entire frontend

C. Results Analysis

Measurement results show that the optimal PCE regions and the peak PCE value match well with the simulation results, which are acquired from the rectifier in the RF front-end. However, the simulation results and model prediction of PCE for a pure rectifier are higher, as shown in Fig. 7(b). That is because, in a real tag environment, the rectifier works along with the ESD protection devices and the demodulator. At -17 dBm, the equivalent power losses brought by them are 1.5 dB, which is equal to approximately 11% degeneration of PCE.

In Table II, we make a comparison with the recent studies using two major $V_{\rm th}$ compensation techniques: static and dynamic. This brief distinguishes itself with a high peak PCE value at the lowest power level.

V. Conclusions

This brief has proposed the analysis and design of a high-efficiency RF front-end for an electronic-product-code Gen2-compatible RFID tag. We construct a steady-state model for a rectifier. The mechanism how W/L, N, V_p, and R_L affect the output voltage and the optimal region of PCE is given through the model. Design instructions for the rectifier are also proposed. The RF front-end is implemented in the RFID tag. This brief serves as a meaningful attempt to help the analysis and design of differential RF fronted for RFID tags.

REFERENCES

[1] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.

[2] S. Mandal and R. Sarpeshkar, "Low-power CMOS rectifier design for RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 6, pp. 1177–1188, Jun. 2007.

[3] X. Wang, B. Jiang, W. Che, N. Yan, and H. Min, "A high efficiency AC–DC charge pump using feedback compensation technique," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 12–14, 2007, pp. 252–255.

[4] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.

[5] A. Facen and A. Boni, "Power supply generation in CMOS passive UHF RFID tags," in *Proc. IEEE Conf. Res. Microelectron. Electron.*, 2006, pp. 33–36.

[6] T.-W. Yoo and K. Chang, "Theoretical and experimental development of 10 and 35 GHz rectennas," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 6, pp. 1259–1266, Jun. 1992.

[7] A. Sasaki and T. Ito, "Differential-drive CMOS rectifier for UHF RFIDs with 66% PCE at −12 dBm input," in *Proc. Tech Papers A-SSCC*, Nov. 2008, pp. 105–108.

[8] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, and K. Gotoh, "A passive UHF RFID tag LSI with 36.6% efficiency CMOS-only rectifier and current-mode demodulator in 0.35 μm FeRAM technology," in *Proc. IEEE Int. Solid-State Circuits*, 2006, pp. 1201–1210.

[9] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuit with self-$V_{\rm th}$-cancellation and power regulation functions for UHF RFIDs," in *Proc. IEEE ASSCC*, Nov. 2007, pp. 119–122.

[10] W. Liu, X. Jin, X. Xi, J. Chen, M.-C. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P. K. Ko, and C. Hu, "BSIM3v3.3 MOSFET model users' manual," Dept. Elect. Eng. Comput. Sci., Univ. California, Berkeley, CA, Tech. Rep. UCB/ERL M98/51, 1998.